Design of AND and NAND Logic Gate Using NDR-BASED Circuit Suitable for CMOS Process

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***Abstract*—AND and NAND logic gate based on the negative differential resistance (NDR) device is demonstrated. This NDR device is made of metal-oxide-semiconductor field-effect-transistor (MOS) devices that could exhibit the NDR characteristic in the current-voltage curve by suitably arranging the MOS parameters. The devices and circuits are implemented by the standard 0.35μm CMOS process.**

I. INTRODUCTION

In the past years, the applications based on negative differential resistance (NDR) devices are of current interest because they are expected to reduce circuit complexity and reach high speed operation integrated circuits [1]-[2]. Some applications make use of the monostable-bistable transition logic element (MOBILE) as a highly functional logic gate [3]-[4]. A MOBILE consists of two NDR devices connected in series and is driven by a bias voltage. The voltage at the output node between the two NDR devices holds on one of the two possible stable states (low and high, corresponding to "0" and "1"), depending on the relative magnitude of peak current of two NDR devices.

The modulation of the NDR's peak current can be controlled by the gate voltage of a MOS device which is connected in parallel with the NDR device. Therefore, we can obtain the logic operation by controlling the switching sequence of the series-connected NDR devices. The AND and NAND logic applications are implemented by the the standard 0.35μm CMOS process.

II. DEVICE STRUCTURE AND OPERATION

The NDR device used in this paper is made of MOS devices, so we regard this NDR device as MOS-NDR device [5]-[6]. Fig. 1 shows the configuration of a MOS-NDR device, which is composed of three NMOS devices and one PMOS device. This circuit is derived from a Λ-type topology described in ref. [7]. The gate of mn3 is connected to the output of the inverter formed by mn1 and mn2. The device mn1 operates as a load resistor. It is used to modulate the gate voltage of mn3. The mn2 behaves as an active switch with the gate connected to the drain of the mn3. The mp4 is used to modulate the I-V characteristic of the MOS-NDR device from Λ type to N type.

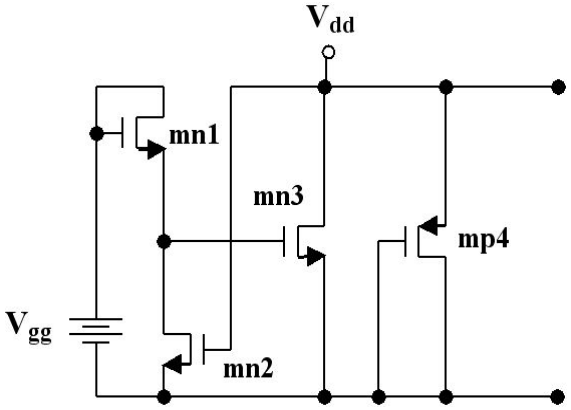

Fig. 1 The circuit configuration for a MOS-NDR device.

This MOS-NDR device can exhibit various NDR current-voltage (I-V) characteristics by choosing appropriate parameters for transistors. The peak current of the NDR I-V characteristics can be adjustable by modulating the Vgg values. Fig. 2 shows the simulated I-V characteristics by modulating the Vgg values from 1.5V to 3.3V, gradually. The length parameters of four MOS are all fixed at 0.35μm. The width parameters of the MOS devices are described as Wmn1=5μm, Wmn2=100μm, Wmn3=10μm, and Wmp4=100μm.

Fig. 3 shows the circuit with the parallel connection of a NMOS and a MOS-NDR device. If the V_G is bigger than the threshold voltage V_T of the NMOS, the total current I_{TOTAL} will be the sum of the currents through the MOS-NDR and NMOS devices. Since the I_{MOS} will be increased with increasing the V_G. Therefore, the I_{TOTAL} will be proportional to the magnitude of the input voltage V_G. It means that we can modulate the peak current of the circuit.

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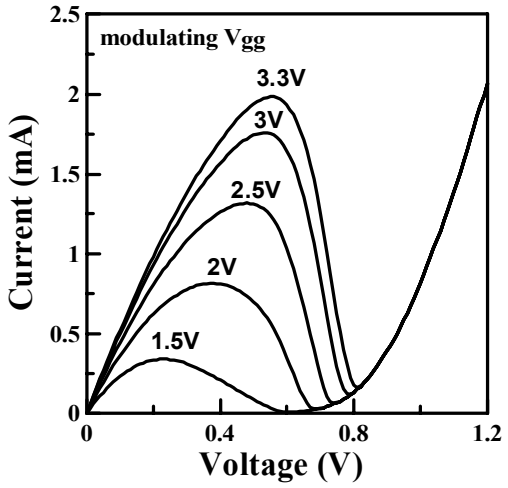

Fig. 2 The Hspice simulated I-V characteristic for a MOS-NDR device by modulating the Vgg values from 1.5V to 3.3V.

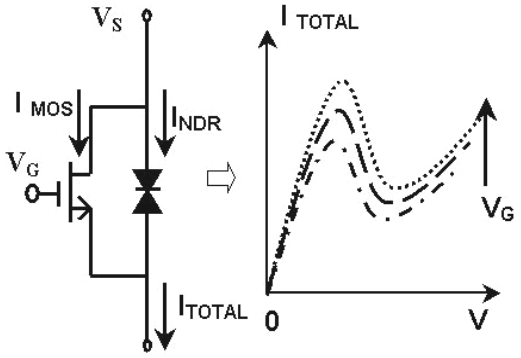

Fig. 3 The peak current of MOS-NDR device could be controlled by the V_G voltage.

III. Logic Circuit Design

Our logic circuit design is based on the MOBILE theory. A MOBILE circuit consists of two NDR devices connected in series and is driven by a bias voltage V_S. Fig. 4 shows the programmable logic circuit. T1 to T4 gates are used as the control gates or the input signal gates. For the AND gate operation, the T1 and T2 are used as the input gates. As for the NAND gate operation, the T3 and T4 are used as the input gates.

The upper NDR1 device is treated as a load device to the pull-down NDR2 driver device. The stable operating point can be determined by the intersection point of two I-V characteristics with the load-line analysis [8], as demonstrated in Fig. 5. The load line, represented by the dashed lines, is the I-V characteristic of upper NDR device. The I-V characteristic of driver device is shown by the solid lines. When the bias voltage is smaller than twice the peak voltage ($2V_P$), there is only one stable point (monostable) in the series circuit, as shown in Fig.5(a). However when the bias voltage is larger than $2V_P$ but smaller than two valley voltages ($2V_V$), there will be two possible stable points (bistable) that respect the low and high states (corresponding to "0" and "1"), respectively. A small difference between the peak currents (I_P) of the NDR1 and NDR2 devices determines the state of the circuit.

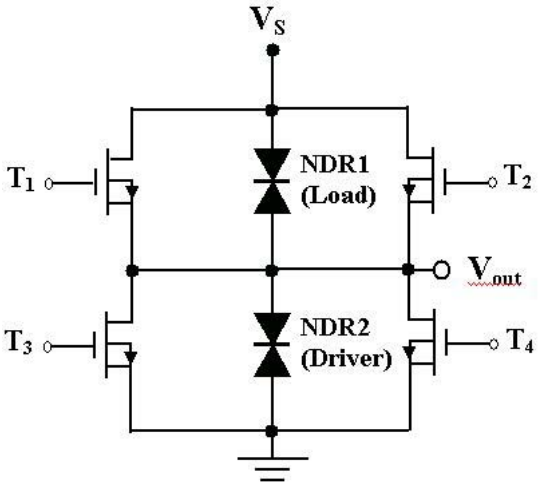

Fig. 4 The circuit configuration of the logic circuit.

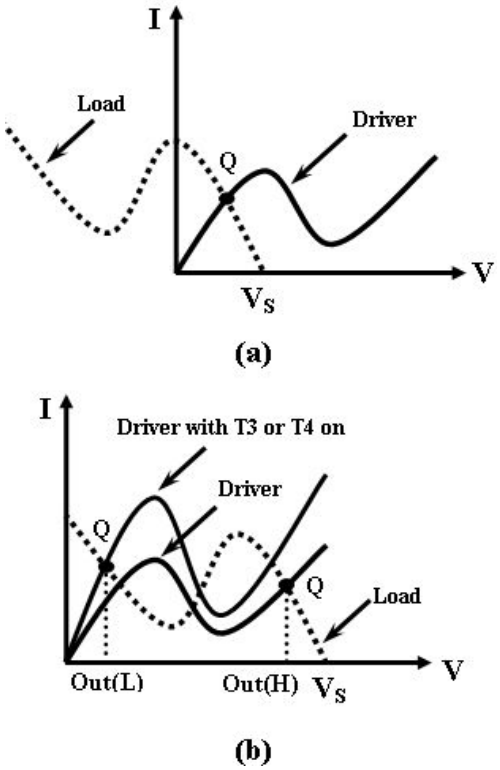

Fig. 5 The load-line analysis for the (a) monostable case (V_S<$2V_P$), (b) bistable case.

If the driver's I_P is smaller than the load's I_P, the circuit switches to the stable point Q corresponding to a high output voltage, as shown in Fig. 5(b). On the other hand, a bigger driver's I_P will result in the low-state operating point Q. After this monostable-to-bistable transition, the output state of the circuit is determined by a small difference in the peak currents of the load and driver MOS-NDR devices.

The load-line analysis for the operation of a AND gate is demonstrated in Fig. 6. Firstly, the I_P of NDR1 must be smaller

than that of NDR2. When the T1 and T2 gates input low, the operating point will be located at Q1. The output voltage will be "low" level. If one of T2 and T3 gates input high, the I_P of I_{TOTAL} will be still smaller than that of NDR2. Then the operating point Q2 will be still located at the relatively "low" level. Only when both T1 and T2 gates input high, the I_P of I_{TOTAL} should be bigger than that of NDR2. Then the operating point Q3 will be located at the "high" level. As for NAND gate operation, the load-line analysis is shown in Fig. 7. The load-line analysis procedure is similar to the AND gate operation. Q1 and Q2 represent the high state, and Q3 demonstrates the low state.

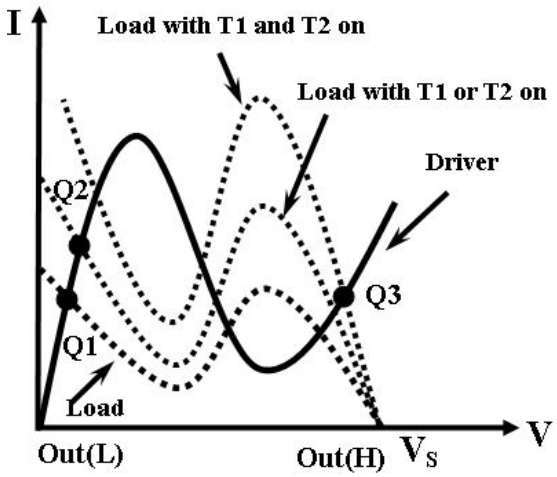

Fig. 6 The load-line analysis for the AND gate

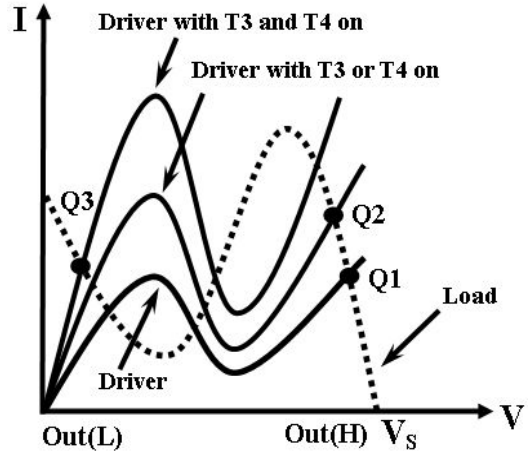

Fig. 7 The load-line analysis for the NAND gate.

IV. RESULTS

The MOS-NDR devices and logic circuits are simulated and fabricated based on the standard 0.35μm CMOS process. The length parameters for all MOS are fixed at 0.35μm. The parameters of the two MOS-NDR devices are designed as Wmn1=5μm, Wmn2=100μm, Wmn3=10μm, and Wmp4=100μm. The width parameters for the T1 to T4 gates are fixed at 5μm. The supply voltage V_S is fixed at 1.4V.

When a MOS-NDR device is connected with a T1 NMOS in parallel, the total current I_{TOTAL} will be the sum of the currents through the MOS-NDR and NMOS devices. Fig. 8 shows the measured I-V characteristics by modulating the T1 voltages gradually. As a result, total current I_{TOTAL} can be controlled efficiently by the T1 gate voltage.

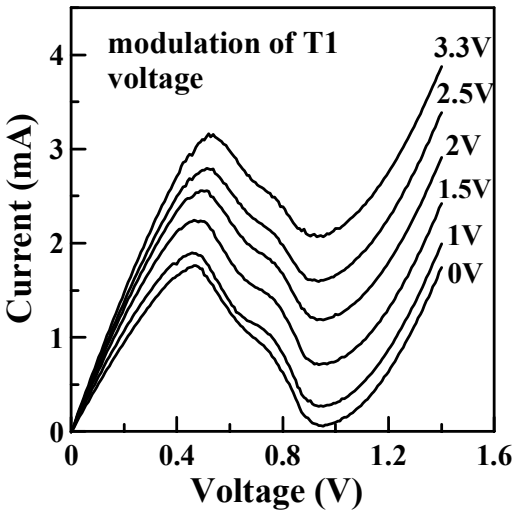

Fig. 8 The peak current of the NDR I-V curve can be controlled by the magnitude of T1 voltage

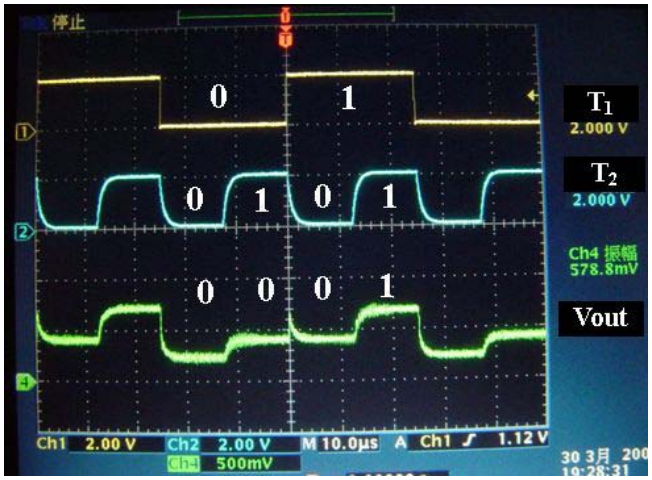

Fig. 9 The measured result for the AND gate operation.

For the AND gate operation, T1 and T2 gates are the input square wave with signal varied from 0 to 2V. The period of T1 is two times of the period of T2 signal. During suitably arranging the parameters, the AND gate operation is shown in Fig. 9. As seen, only when two input gates are high, the output voltage is located at relatively "high" level.

For the NAND gate operation, T3 and T4 gates input signal. Fig. 10 demonstrates the NAND gate operation of the MOBILE circuit. As shown, only when two input gates are high, the output voltage is located at relatively "low" level.

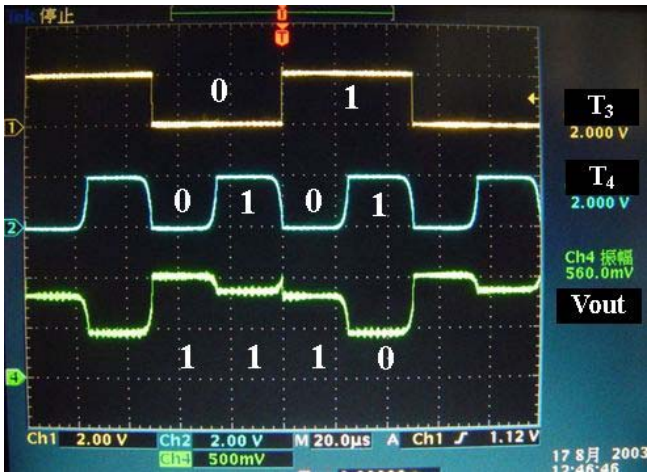

Fig. 10 The measured result for the NAND gate operation.

V. CONCLUSIONS

We have fabricated the MOS-NDR device based on the standard 0.35µm CMOS process. We also have demonstrated the AND and NAND logic applications based on the MOS-NDR devices.

Most of the previously published NDR-based applications are utilized the resonant tunneling diode (RTD) as the basic element. The fabrication of such RTD devices and circuits is based on the molecular-beam-epitaxy (MBE) or metal-organic-chemical-vapor-deposition (MOCVD) technique, which are not compatible with main stream Si-based CMOS or SiGe-based BiCMOS process. The MOS-NDR device is composed of MOS devices, yet it is much more convenient to combine with other devices and circuits to achieve the system-on-a-chip (SoC) by the standard CMOS or BiCMOS process.

VI. ACKNOWLEDGMENTS

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VII. REFERENCES

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